LYNXAR
Everything programmable

**Data Sheet**

DeviceClip Platform
**DC4S**


## DeviceClip platform DC4S main features

- ✓ 4 independent ISP channels (targets)
- ✓ 6 data signals per channel
- ✓ Relay isolation barrier on all channels

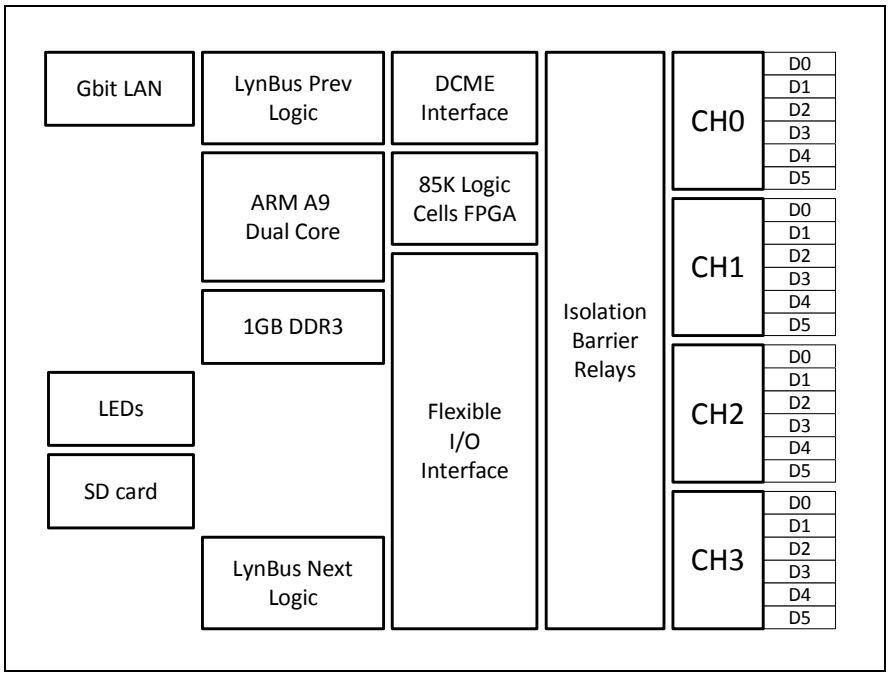
## DeviceClip architecture overview

DeviceClip is a hi-performance, professional, universal, modular platform for the in-system programming of every type of semiconductor devices (microcontrollers, serial memories, PLDs from every semiconductor producer). It is provided of a number of true-parallel channels for the simultaneous support of totally different (heterogeneous) devices.

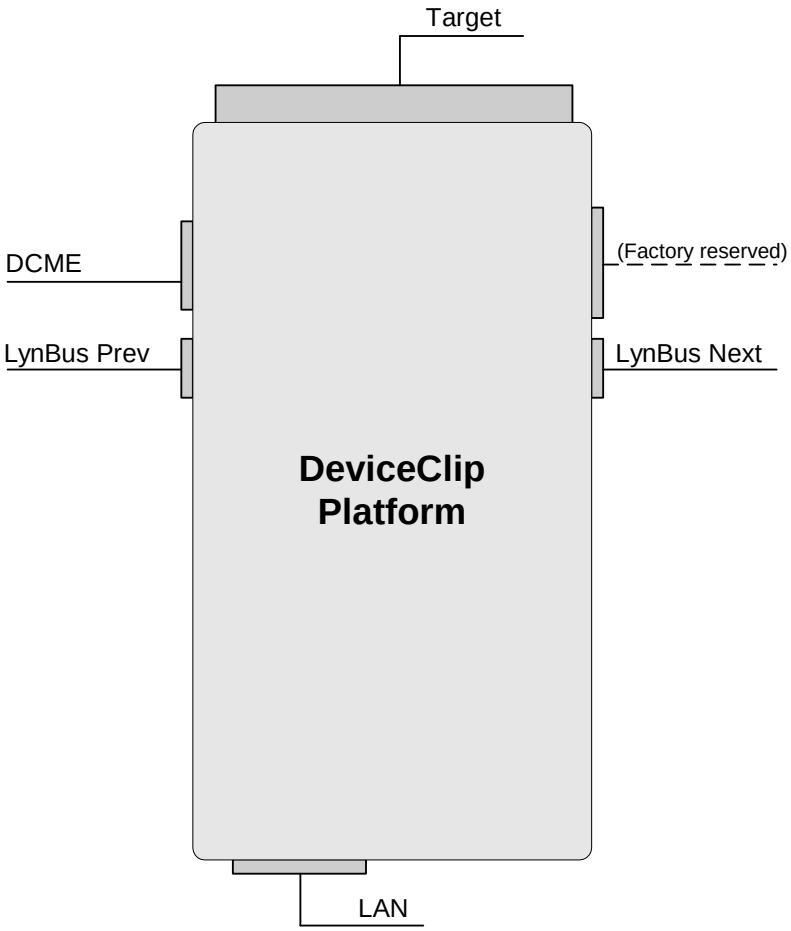
Unlike other programming tools, DeviceClip was conceived to work from inside the test fixture. Compact size allows placement at very short distance from the device to be programmed, dramatically reducing signal noise and allowing the target device maximum speed to be achieved.

Thanks to its ultra-high speed and unlimited number of truly parallel channels, DeviceClip offers the market most competitive cost of operation when supporting panels of PCBAs.

## Block diagram



## Platform connectors




**Target** ISP data signals for target device(s) and DeviceClip power. Pin assignments are on the specific section below.

**LynBus Next** This connector allows cascading of more DeviceClip platforms to form a larger than one unit programming system. See DeviceClip Architecture User's Manual for details.

**LAN** This connector allows an RJ-45 host LAN to be linked through DCLA adapter provided on DeviceClip ToolBox.

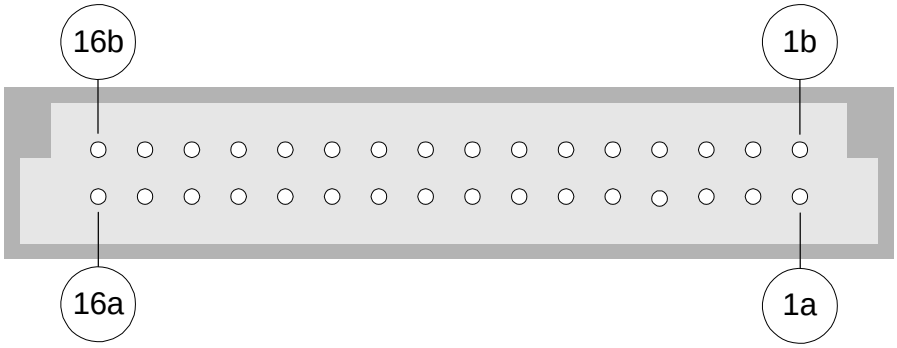
**LynBus Prev** This connector allows cascading of more DeviceClip platforms to form a larger than one unit programming system. See DeviceClip Architecture User's Manual for details.

**DCME** This connector allows the connection of a Lynxar Technologies DCME module. See DeviceClip Architecture User's Manual for details.

## Target connector

DeviceClip Target connector is a standard DIN41612 32-pin header (rows a-b). It carries ISP data signals and also conveys power supply to the platform. The following figure shows the Target connector pin assignment.

| Pin | Row a | Row b |
|---|---|---|
| 1 | CH0_D0 | CH0_D1 |
| 2 | CH0_D2 | CH0_D3 |
| 3 | CH0_D4 | CH0_D5 |
| 4 | GND | GND |
| 5 | CH1_D0 | CH1_D1 |
| 6 | CH1_D2 | CH1_D3 |
| 7 | CH1_D4 | CH1_D5 |
| 8 | CH2_D0 | CH2_D1 |
| 9 | CH2_D2 | CH2_D3 |
| 10 | CH2_D4 | CH2_D5 |
| 11 | GND | GND |
| 12 | CH3_D0 | CH3_D1 |
| 13 | CH3_D2 | CH3_D3 |
| 14 | CH3_D4 | CH3_D5 |
| 15 | **GND** | **GND** |
| 16 | **POWER** | **POWER** |




On this table, four-channel target ISP signals are represented as CHc_Ds, where ‘c’ is the channel number and ‘s’ is the data signal for the related channel. When implementing DeviceClip on your application, make sure to connect POWER to a VCC voltage.

A mating wire-wrap connector is included on DeviceClip platform package and can be used to join the Target connector signals to the nails of your test fixture.

DeviceClip platform series can be installed in common, wire-wrap fixtures or in wireless fixtures. Suggested mating connector for the two options are:

| | Wire-wrap fixture | Wireless fixture |
|---|---|---|
| **Manufacturer** | Conec | Hirose |
| **Manufacturer P/N** | 122 A 10439 X | PCN10C-32S-2.54DS(72) |
| **Digi-Key P/N** | 122A10439X-ND | H11170-ND |

## General characteristics

| Item | Min | Typ | Max | Units |
|---|---|---|---|---|
| Processor operating frequency (Dual-core ARM® Cortex™-A9) | | 667 | | MHz |
| SDRAM (DDR3L) size | | 1 | | GB |
| SDRAM (DDR3L) performance | | 1.066 | | GB/s |
| Storage memory (Micro SDHC card) | 4 | 8 | 32 | GB |
| Supply voltage | 6 | 12 | 16 | V |
| Power consumption | | 3.6 | | W |
| Peak current (@12V) | | 1.7 | | A |
| Length | | 107 | | mm |
| Width | | 60 | | mm |
| Height | | 10 | | mm |
| Weight | | 70 | | g |
| Operational temperature | | 5-70 | | °C |

## Channel description

DeviceClip model DC4S is provided of 4 channels (CH0-CH3).
Each of DeviceClip model DC4S channels is provided of 6 data signals (D0-D5).

Data signals, depending on the target device being managed, are configured by Applications in one of the following modes:

| Mode | Mode name | I/O type | Applicable |
|---|---|---|---|
| 0 | High impedance (Z) | Z | D0-D5 |
| 1 | Digital input | IN | D0-D5 |
| 2 | Digital input (3.3KΩ pull-up) | IN | D0-D5 |
| 3 | Push-pull digital output | OUT | D0-D5 |
| 4 | Open drain digital output | OUT | D0-D5 |
| 5 | Open drain digital output (3.3KΩ pull-up) | OUT | D0-D5 |
| 6 | Clock digital push-pull output | OUT | D0-D5 |
| 7 | High voltage | VPP | D0 |

Note: Target data signals voltage ($VCC_{TIO}$) is programmable and ranges from 1.56V to 5.04V.

## Electrical characteristics (mode 0)

Maximum leakage current (@25°C): 2uA.

## Electrical characteristics (modes 1-2)

| $VCC_{TIO}$ | $V_{IL}$ | $V_{IH}$ | Unit |
|---|---|---|---|
| 1.65 to 1.95 | $VCC_{TIO}$ * 0.35 | $VCC_{TIO}$ * 0.65 | V |
| 2.3 to 2.7 | 0.7 | 1.7 | V |
| 3.0 to 3.6 | 0.8 | 2.0 | V |
| 4.5 to 5.5 | $VCC_{TIO}$ * 0.30 | $VCC_{TIO}$ * 0.70 | V |

## Electrical characteristics (modes 3-6)

| $VCC_{TIO}$ | $V_{OL}$ | $V_{OH}$ | Unit |
|---|---|---|---|
| 1.65 | 0.45 @4mA | 1.20 @-4mA | V |
| 2.3 | 0.30 @8mA | 1.90 @-8mA | V |
| 3 | 0.55 @24mA | 2.40 @-24mA | V |
| 4.5 | 0.55 @32mA | 3.80 @-32mA | V |

## Electrical characteristics (mode 7)

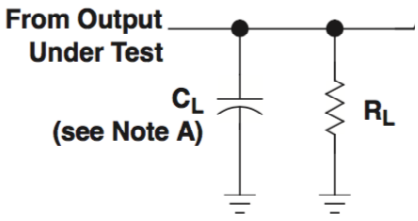
VPP voltage is programmable and ranges from 4.96V to 15.80V, +/-5 % (granularity: 42mV).

## Absolute maximum ratings

| Signal | Min | Max | Unit |
|---|---|---|---|
| POWER | -50 | 20 | V |
| Data signals | -24 | $VCC_{TIO}$ + 24 | V |

## Swithing characteristics

Test conditions ($R_L$ = 2kΩ, $C_L$ = 15pF)




Note A: CL includes probe and jig capacitance.

| $VCC_{TIO}$ | Rise Time (min) | Rise Time (max) | Fall Time (min) | Fall Time (max) | Unit |
|---|---|---|---|---|---|
| 1.8 | 2.7 | 4.6 | 1.5 | 2.6 | ns |
| 2.5 | 1.8 | 1.9 | 1.5 | 1.7 | ns |
| 3.3 | 0.9 | 1.6 | 0.9 | 1.5 | ns |
| 5 | 1.5 | 2.5 | 1.0 | 1.8 | ns |

## DeviceClip architecture available literature

- Architecture Overview Brochure
- Architecture User's Manual
- Platforms Data Sheets
- Apps (programming algorithms) Data Sheets

Document code: **DC02058**


**www.lynxar.us**